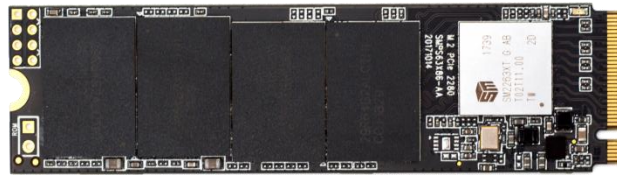


ALFAMEMORY M.2 PCIe 2280 DATASHEET

M.2 PCIe 2280 SOLID STATE DRIVE



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1.0 PRODUCT DESCRIPTION

1.1 PRODUCT OVERVIEW

PCIe as a storage protocol is designed from the ground up to work with non-volatile memory (NVM), including the current NAND flash technology and next-generation NVM technologies. As such, it does not have the same limitations as storage protocols designed for hard disk drives.

Alfamemory M.2 PCIe SSD is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 3.1 interface standard up to 4 lanes shows much faster performance than previous SSDs. Alfamemory M.2 PCIe provide more performance in terms of bandwidth and lower latency than SAS and SATA based counterparts.

1.2 TARGET APPLICATIONS

- Military and Aerospace
- Embedded / Industrial Systems
- Medical Industry
- Notebook
- Casino Gaming

1.3 PRODUCT FEATURES

- Native-PCIe SSD with 2x Core ARM Cortex processor (SM226x family)
- Capacity: 128GB, 256GB, 512GB, 1TB
- PCI Express Gen3: Single port X4 lanes
- Compliant with PCI Express Base Specification Rev. 3.1
- Compliant with NVM Express Specification Rev.1.3
- Static and Dynamic Wear Leveling and Bad Block Management
- Support up to queue depth 64K
- Max. ECC of 2KB LDPC + RAID
- Support for Toggle
- Reliable TLC NAND type flash
- Support SMART and TRIM commands
- 100% tested HW and SW

1.4 SYSTEM REQUIREMENTS

Operating Voltage Requirement: $V_{cc} = 3.3V \pm 5\%$

Operating System: Supported by all operating systems

Interface: Socket 3 (M key)

Installation Requirements:

- System Hardware which supports Socket 3 (M key) standards
- System Hardware includes M.2 socket or transfer board

2.0 PRODUCT ORDERING PART NUMBERS

2.1 ORDERING PART STRUCTURE

Table 1: Ordering Part Structure

<u>Prefix</u> X	<u>Product</u> XX	<u>Controller</u> XX	<u>Density</u> XXXX	<u>Flash Comp.</u> XX	<u>Temp. & Remark</u> X
A	PB- PCIe Gen 3 NVMe M.2 2282	SC-SM2263XT	128G - 128GByte 256G - 256GByte 512G - 512GByte 001T - 1TByte	XT – 3D TLC	C-Commercial

2.2 VALID ORDERING PART NUMBERS

Table 2: Valid Ordering Part Numbers

Product Family	Capacity	Flash	Form Factor	Part Number
M.2 PCIe	128GB	TLC	M.2 2280	APBSC128GXTC
	256GB			APBSC256GXTC
	512GB			APBSC512GXTC
	1TB			APBSC001TXTC

3.0 PHYSICAL SPECIFICATIONS

3.1 MECHANICAL SPECIFICATIONS(PCBA)

Length: 80.0 ± 0.15 mm

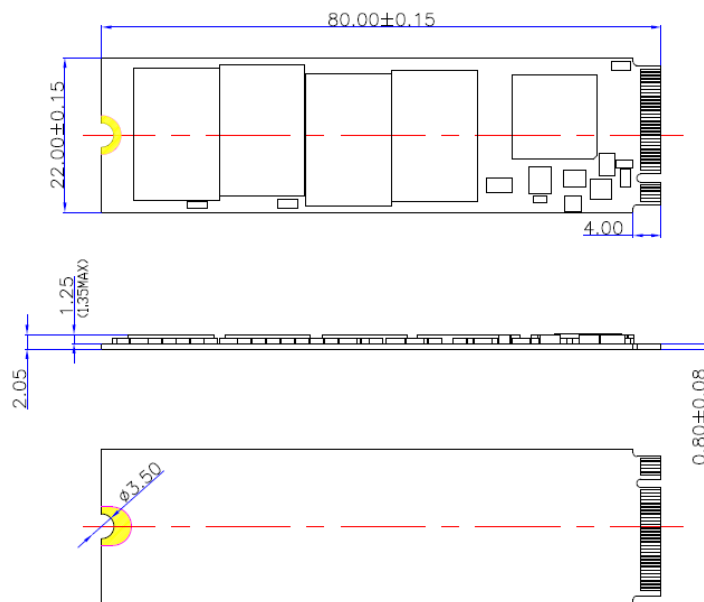
Width: 22.0 ± 0.15 mm

PCB Thickness: 0.80 ± 0.08 mm

TOP Thickness: Max to 1.35 mm

Weight: <7.0g

Figure 1:M.2 PCIe 2280 Outline Drawing



4.0 ELECTRICAL SPECIFICATIONS

Operating Voltage: $V_{CC} = 3.3V \pm 5\%$

Modes: PCIe 3.0

4.1 PERFORMANCE SPECIFICATIONS

Access Time: 0.2 ms

Seek Time: 0 ms

Mount Time: Dependent on system HW and SW

Power on to Ready: Dependent on system HW and SW

Data Transfer Time: Rated Data Transfer Speeds are maximums based on Crystal Disk Mark

* M.2 Port and the installation of an enhanced driver required for maximum speed

Table 3: Data Transfer Time Specifications

Device	Sequential Read Max (MB/Sec)	Sequential Write Max (MB/Sec)
APBSC128GXTC	1800	570
APBSC256GXTC	1900	1000
APBSC512GXTC	2000	1600
APBSC001TXTC	2100	1700

4.2 POWER AND TEMPERATURE CONDITIONS

Table 4: Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	-0.3 to +3.6	V
V_{IN}	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage Temperature	-45 to 85	°C
T_{OPR}	Commercial Grade	0 to +70	°C

4.3 POWER CONSUMPTION TEST FOR RESULT

Table 5: Power Consumption

Capacity	Product status(W)		
	Idle	Read	Write
128GB	1.51	2.13	2.22
256GB	1.57	1.86	2.3
512GB	1.56	1.86	2.26
1TB	2.07	2.3	2.31

4.4 TOTAL BYTES WRITTEN

Table 6:TBW and Daily Usage Guideline results

Capacity	TBW	Daily Usage Guideline
128GB	50TB	45GB/day
256GB	100TB	90GB/day
512GB	200TB	180GB/day
1TB	400TB	360GB/day

TBW: Total Bytes Written (TBW according to flash)

Definition and conditions of TBW are based on JEDEC standard

Daily usage guidelines value is calculated by dividing TBW by 365*3

5.0 ENVIRONMENTAL SPECIFICATIONS

Operating Temperature:

Commercial Grade: 0°C to +70°C

Humidity: humidity at 60%, at 50 °C for 48 hours.

Operating Vibration:

Frequency/Displacement: 20~80Hz/1.52mm.

Frequency/Acceleration: 80~2000Hz/20G.

Axis: X, Y, Z axis. 60min/Axis.

6.0 QUALITY AND RELIABILITY SPECIFICATIONS

Data Retention: JESD47 compliant

Wear Leveling: Dynamic and static wear-leveling

Bad Block Management: Drive will self identify bad blocks and remap physical to logical addresses to avoid bad blocks

ECC/EDC (Error Correction Code/Error Detection Code): Built in error detection and correction will correct physical bit errors in NAND. Drives use Max. ECC of 2KB LDPC + RAID.

MTBF: >1,000,000 hours

Power Cycle: 1000 times

7.0 COMPLIANCE SPECIFICATIONS

All NVMe are compliant with the following standards and regulations:

- RoHS
- CE
- FCC

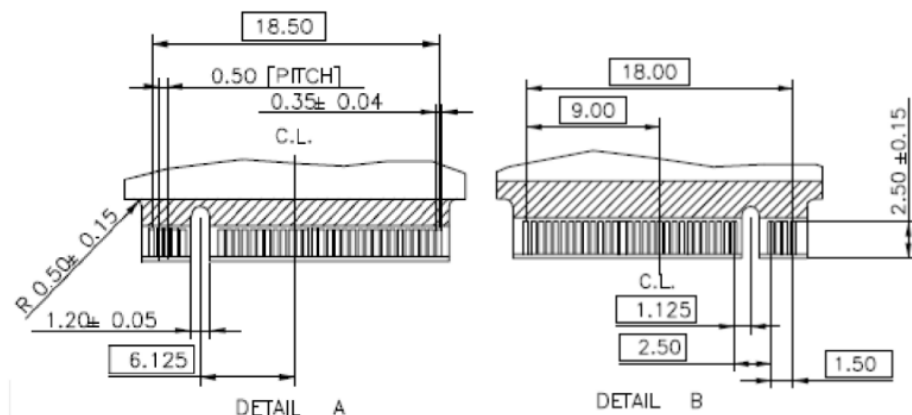
8.0 PIN DESCRIPTIONS

8.1 M.2 INTERFACE DRAWING

Interface Description (M Key)

Figure 2: M.2 Interface Description

M.2 PCIe 2280 Datasheet



8.2 PIN SIGNALS ASSIGNMENTS

Table 7: Pin Assignment

1	GND	Return Current Path	2	+3.3V	3.3V Power (Source)
3	GND	Return Current Path	4	+3.3V	3.3V Power (Source)
5	PETn3	PCIe TX	6	N/A	Reserved
7	PETp3	PCIe TX	8	N/A	Reserved
9	GND	Return Current Path	10	LED1#	Device Activity Signal
11	PERn3	PCIe RX	12	+3.3V	3.3V Power (Source)
13	PERp3	PCIe RX	14	+3.3V	3.3V Power (Source)
15	GND	Return Current Path	16	+3.3V	3.3V Power (Source)
17	PETn2	PCIe TX	18	+3.3V	3.3V Power (Source)
19	PETp2	PCIe TX	20	N/A	Reserved
21	GND	Return Current Path	22	N/A	Reserved
23	PERn2	PCIe RX	24	N/A	Reserved
25	PERp2	PCIe RX	26	N/A	Reserved
27	GND	Return Current Path	28	N/A	Reserved
29	PETn1	PCIe TX	30	N/A	Reserved
31	PETp1	PCIe TX	32	N/A	Reserved
33	GND	Return Current Path	34	N/A	Reserved
35	PERn1	PCIe RX	36	N/A	Reserved
37	PETp1	PCIe RX	38	N/A	Reserved
39	GND	Return Current Path	40	N/A	Reserved
41	PETn0	PCIe TX	42	N/A	Reserved
43	PERp1	PCIe TX	44	N/A	Reserved
45	GND	Return Current Path	46	N/A	Reserved
47	PERn0	PCIe RX	48	N/A	Reserved
49	PERp0	PCIe RX	50	PERST#	PCIe Reset

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51	GND	Return Current Path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	Reserved
55	REFCLKP	PCIe Reference Clock	56	N/A	Reserved
57	GND	Return Current Path	58	N/A	Reserved
59	Notch	M Key	60	Notch	M Key
61	Notch	M Key	62	Notch	M Key
63	Notch	M Key	64	Notch	M Key
65	Notch	M Key	66	Notch	M Key
67	N/A	Removed	68	SUSCLK	Reserved
69	PEDET	Removed	70	+3.3V	3.3V Power (Source)
71	GND	Return Current Path	72	+3.3V	3.3V Power (Source)
73	GND	Return Current Path	74	+3.3V	3.3V Power (Source)
75	GND	Return Current Path			

9.0 PCIE AND NVM EXPRESS REGISTERS

9.1 PCI EXPRESS REGISTERS

M.2 supports the command show in the following tables.

Table 8: Register Summary Table

Description	Start Address	End Address	Protocol
PCI Register Summary			
PCI Header	00h	3Fh	PCI Capability
PCI Power Management Capability	40h	47h	PCI Capability
MSI Capability	50h	67h	PCI Capability
PCI Express Capability	70h	A3h	PCI Capability
MSI-X Capability	80h	BBh	PCI Capability
Advanced Error reporting Capability	100h	12Bh	PCI Capability
Device Serial NO Capability	148h	157h	PCI Capability
Power Budgeting Capability	158h	167h	PCI Capability
Secondary PCI Express Header	168h	17Bh	PCI Capability
Latency Tolerance Reporting(LTR)	188h	18Fh	PCI Capability
L1 Substates Capability Register	190h	19Fh	PCI Capability
PCI Header Register Summary			
Identifiers	00h	03h	ID
Command Register	04h	05h	CMD
Device Status	06h	07h	STS
Revision ID	08h	08h	RID
Class Codes	09h	0Bh	CC
Cache Line Size	0Ch	0Ch	CLS

Description	Start Address	End Address	Protocol
Master Latency Timer	0Dh	0Dh	MLT
Header Type	0Eh	0Eh	HTYPE
Built in Self Test	0Fh	0Fh	BIST
Memory Register Base Address (lower 32-bit)	10h	13h	MLBAR (BAR0)
Memory Register Base Address (upper 32-bit)	14h	17h	MUBAR (BAR1)
Index/Data Pair Register Base Address	18h	1Bh	IDBAR (BAR2)
Reserved	1Ch	1Fh	BAR3
Reserved	20h	23h	BAR4
Reserved	24h	27h	BAR5
CardBus CIS Pointer	28h	2Bh	CCPTR
Subsystem Identifiers	2Ch	2Fh	SS
Expansion ROM Base Address	30h	33h	EROM
Capabilities Pointer	34h	34h	CAP
Reserved	35h	3Bh	R
Interrupt Information	3Ch	3Dh	INTR
Minimum Grant	3Eh	3Eh	MGNT
Maximum Latency	3Fh	3Fh	MLAT
PCI Power Management Capability Register Summary			
PCI Power Management Capability ID	40h	40h	PID
Next cap ptr	41h	41h	Next cap ptr
PC Power Management Capabilities	42h	43h	PMC
PCI Power Management Control and Status	44h	45h	PMCS
PMCSR_BSE Bridge Extensions	46h	46h	PMCSR_BSE
Data	47h	47h	Data
PCI Express Capability Register Summary			
Description	Start Address	End Address	Symbol
PCI Express Capability ID	70h	71h	PXID
PCI Express Capabilities	72h	73h	PXCAP
PCI Express Device Capabilities	74h	77h	PXDCAP
PCI Express Device Control	78h	79h	PXDC
PCI Express Device Status	7Ah	7Bh	PXDS
PCI Express Link Capabilities	7Ch	7Fh	PXLCAP
PCI Express Link Control	80h	81h	PXLC
PCI Express Link Status	82h	83h	PXLS
PCI Express Device Capabilities 2	94h	97h	PXDCAP2
PCI Express Device Control 2	98h	99h	PXDC2
PCI Express Device Status 2	9Ah	9Bh	PXDS2
PCI Express Link Capabilities 2	9Ch	9Fh	PXLCAP2

Description	Start Address	End Address	Protocol
PCI Express Link Control 2	A0h	A1h	PXLC2
PCI Express Link Status 2	A2h	A3h	PXLS2
Advanced Error Reporting Capability Register Summary			
AER Capability ID	100h	103h	AERID
AER Uncorrectable Error Status	104h	107h	AERUCES
AER Uncorrectable Error Mask	108h	10Bh	AERUCEM
AER Uncorrectable Error Severity	10Ch	10Fh	AERUCESEV
AER Correctable Error Status	110h	113h	AERCES
AER Correctable Error Mask	114h	117h	AERCEM
AER Advanced Error Capabilities and Control	118h	11Bh	AERCC
AER Header Log	11Ch	12Bh	AERHL
Secondary PCI Express Capability Register Summary			
Secondary PCI Express Capability	168h	16Bh	SPXID
PCI Express Link Control 3	16Ch	16Fh	PXLC3
PCI Express Lane Error Status	170h	173h	PXLE
PCI Express Lane 0 Equalization Control	174h	175h	PXL0EC
PCI Express Lane 1 Equalization Control	176h	177h	PXL1EC
PCI Express Lane 2 Equalization Control	178h	179h	PXL2EC
PCI Express Lane 3 Equalization Control	17Ah	17Bh	PXL3EC
Secondary PCI Express Capability Register Summary			
Secondary PCI Express Capability	168h	16Bh	SPXID
PCI Express Link Control 3	16Ch	16Fh	PXLC3
PCI Express Lane Error Status	170h	173h	PXLE
PCI Express Lane 0 Equalization Control	174h	175h	PXL0EC
PCI Express Lane 1 Equalization Control	176h	177h	PXL1EC
PCI Express Lane 2 Equalization Control	178h	179h	PXL2EC
PCI Express Lane 3 Equalization Control	17Ah	17Bh	PXL3EC
NVM Express Registers Register Summary			
Controller Capabilities	00h	07h	CAP
Version	08h	0Bh	VS
Interrupt Mask Set	0Ch	0Fh	INTMS
Interrupt Mask Clear	10h	13h	INTMC
Controller Configuration	14h	17h	CC
Reserved	18h	1Bh	Reserved
Controller Status	1Ch	1Fh	CSTS
Reserved	20h	23h	Reserved
Admin Queue Attributes	24h	27h	AQA
Admin Submission Queue Base Address	28h	2Fh	ASQ
Admin Completion Queue Base Address	30h	37h	ACQ

Description	Start Address	End Address	Protocol
Reserved	38h	EFFh	Reserved
Command Set Specific	F00h	FFFh	Reserved
Submission Queue 0 Tail Doorbell (Admin)	1000h	1003h	SQ0TDBL
Completion Queue 0 Head Doorbell (Admin)	1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL
Submission Queue y Tail Doorbell	1000h + (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL
Completion Queue y Head Doorbell	1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQyHDBL

10.0 SUPPORTED COMMAND SET

Table 9: Opcode for Admin Commands

Command Name	Opcode (Hex)
Delete I/O Submission Queue	00h
Create I/O Submission Queue	01h
Get Log Page	02h
Delete I/O Completion Queue	04h
Create I/O Completion Queue	05h
Identify	06h
Abort	08h
Set Feature	09h
Get Feature	0Ah
Asynchronous Event Request	0Ch
Firmware Activate	10h
Firmware Image Download	11h
Not used (I/O Command Set Specific)	80h – BFh
Not used (Vendor Specific)	C0h – FFh
Format NVM	80h
Security Send	81h
Security Receive	82h

Table 10: Identify Command Table Information

Description	Bytes	O/M	Default Value
PCI Vendor ID	1:00	M	tbd
PCI Subsystem Vendor ID	3:02	M	tbd

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Description	Bytes	O/M	Default Value
Serial Number (ASCII), #:Variables	23:04	M	tbd
Model Number (ASCII)	63:24:00	M	(see PN table)
Firmware Revision, #:Variables	71:64	M	tbd
Recommended Arbitration Burst	72	M	tbd
IEEE OUI	75:73	M	tbd
Controller Multi-Path I/O and Namespace Sharing Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port	76	O	tbd
Maximum Data Transfer Size Bit 0: 1h - Supported (dual port - future value) 0h - Not Support (Single Port) Maximum Data Transfer Size (MDTS)	77	M	tbd
Controller ID (CNTLID)	79:78	M	tbd
Reserved	255:80	M	tbd
Optional Admin Command Support Bits 15:3 - Reserved Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported (PM953 conditionally supports the Namespace Management and Namespace Attachment command(NVMe v1.2 specification) for reconfigurable overprovisioning) Bit 2: 1h - Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported	257:256	M	tbd
Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)	258	M	tbd
Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)	259	M	tbd
Firmware Updates Bits 7:4 - Reserved Bits 3:1 - Number of firmware slots Bit 0 - 1h Slot 1 is read only	260	M	tbd
Log Page Attributes Bits 7:1 - Reserved Bit 0: 0h SMART data is global for all namespaces	261	M	tbd

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Description	Bytes	O/M	Default Value
Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)	262	M	tbd
Number of Power States Support (0's based value)	263	M	tbd
Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.0c Figure 8	264	M	tbd
Autonomous Power State Transition Attributes (APSTA)	265	O	tbd
Reserved	511:266	-	-
Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)	512	M	tbd
Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)	513	M	tbd
Reserved	515:514	-	tbd
Number of Namespaces	519:516	M	tbd
Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare	521:520	M	tbd
Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported	523:522	M	tbd
Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase Per Namespace Bit 0 – 0h Format Per Namespace	524	M	tbd
Volatile Write Cache 0h – No VWC present	525	M	tbd
Atomic Write Unit Normal	527:526	M	tbd

Description	Bytes	O/M	Default Value
Atomic Write Unit Power Fail (0's based value)	529:528	M	tbd
NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express 1.1.a	530	M	tbd
Reserved	531	M	tbd
ACWU	533:532	O	tbd
Reserved	534:533	M	tbd
No SGL support	539:536	O	tbd
Reserved	703:540	-	tbd
Reserved	2047:704	-	tbd
Power State 0 Descriptor	2079:2048	M	refer to 'Identify Power State Descriptor Data Structure'
N/A	2111:2080	O	tbd
N/A	2143:2112	O	tbd
N/A	-	-	tbd
Power State 31 Descriptor (N/A)	3071:3040	O	tbd
Reserved	4095:3072	1	-

11.0 INSTALLATION

BEFORE GETTING STARTED

1. Back Up Your Data

VISUAL INSPECTION

1. Before unpacking and handling the SSD, discharge the static electricity by touching the metal chassis of your computer or by using an anti-static wrist strap
2. Inspect the box and device for the following
 - a. Box is damaged or water-stained
 - b. Any damage to the SSD

HANDLING THE SSD

1. Be cautious when unpacking, installing, and handling the SSD drive. Misuse of the SSD voids all warranty. Follow the succeeding instructions when managing the SSD
2. Follow all ESD pre-cautions
3. Always operate the SSD within environmental conditions
4. Never switch DC power to the drive by plugging an electrically live source cable into the drive's power connector

INSTALLATION

System Requirements

To install the SSD in your computer, ensure that you have the following items:

1. Mounting Screws (If needed)

Install the SSD

Follow these steps to install the SSD

1. Power down the PC
2. Remove the computer system outside cover
3. Insert the SSD to the connector on motherboard
4. Replace the PC cover
5. Power on the PC
6. A BIOS sign-on message appears and displays a key sequence to enter the BIOS setup. Set up the BIOS to recognize the SSD.
7. Installation is Complete

USING THE SSD IN A MS-DOS OS

The SSD is already partitioned and formatted by NTFS, so if you want to install MS-DOS O/S on the SSD, it should be re-partitioned and re-formatted. After installing the SSD, it must be installed as a disk drive under DOS. Run the DOS commands as listed below and follow the instructions displayed for each command.

1. Run the DOS FDISK program to partition the SSD
2. Verify that the partition is active and ready for formatting
3. Run the DOS FORMAT command to high-level format the SSD

USING THE SSD IN A WINDOWS OS

No modifications need to be made to use the SSD in a Windows OS platform

USING THE SSD IN A LINUX O/S

Port driver is needed to be made to use the SSD in Linux OS platforms. please contact Alfamemory technical support for more detail.

USING THE SSD IN OTHER O/S

Port driver is needed to be made to use the SSD in other OS platforms. please contact Alfamemory technical support for more detail.

FOR MORE INFORMATION

For Technical Support:

If additional support is needed, please visit the Alfamemory Web site at www.alfamemory.com for the following topics:

- **Warranty Services:** Includes the warranty service policy and the RMA request forms.
- **Technical Information:** Includes product data sheets and various USB whitepapers.
- **Tools Section:** Includes frequently asked questions (FAQs).

For More Information or Further Technical Support Please Contact:

Alfamemory Technology CO., Ltd.

Support: Support@alfamemory.com

CHANGE RECORD

Table 11: Change Record

Version	Release Date	Changes
1.0	Nov 20th, 2018	Initial Release in new template
1.1	Aug 30th, 2019	Revise Power Consumption Testing result
1.2	Jul 1st, 2020	Modify Ordering Part Numbers
1.3	Apr 1 st , 2021	Modify TBW SPEC.